

**ABSTRACT OF THE DISCLOSURE**

A design tool for generating circuit block constraints from a design environment. The design tool derives a fan-in cone function for each block input of a circuit block of a design. The fan-in cone function may include fan-in cone variables and block input variables. The  
5 fan-in cone functions are conjoined into a circuit block constraint functions. The circuit block constraint function is quantified to provide circuit block constraints. These constraints may be used in design verification (e.g. equivalence checking) and/or circuit analysis (e.g. timing rule generation).